1. Product characteristics

ÿ Kernel

— 32-bit ARM® Cortex® - M0+

— Up to 32MHz operating frequency

ÿ Memory

— Maximum 64Kbytes flash memory

— Maximum 8Kbytes SRAM

ÿ Clock system

— Internal 4/8/16/22.12/24MHz RC oscillator (HSI)

— Internal 32.768KHz RC oscillator (LSI)

— 4~32MHz crystal oscillator (HSE)

ÿ Power management and reset

— Working voltage: 1.7V~5.5V

— Low power modes: Sleep and Stop

— Power-on/power-down reset (POR/PDR)

— Brownout detection reset (BOR)

— Programmable Voltage Detection (PVD)

ÿ General-purpose input and output (I/O)

— Drive current 8mA

ÿ 3-channel DMA controller

ÿ 1 x 12-bit ADC

— Supports up to 10 external input channels

— Input voltage conversion range: 0~VCC

ÿ Timer

— 1 16bit advanced control timer (TIM1)

— 4 general-purpose 16-bit timers

(TIM3/TIM14/TIM16/TIM17)

— 1 low-power timer (LPTIM), supports wake-up from stop mode

— 1 independent watchdog timer (IWDT)

— 1 window watchdog timer (WWDT)

— 1 SysTick timer

— 1 IRTIM

ÿRTC

ÿ Communication interface

— 1 serial peripheral interface (SPI)

— 2 Universal Synchronous/Asynchronous Receiver-Transmitter (USART), supporting automatic waveform

Rate detection

— 1 I2C interface, supports standard mode (100kHz), fast mode (400kHz),

supports 7-bit addressing mode

ÿ Hardware CRC-32 module

ÿ 2 comparators

ÿ Unique UID

ÿ Serial Single Wire Debug (SWD)

ÿ Working temperature: -40~85ÿ

ÿ Package SOP16

Table of contents

2. Introduction

PY32F003 series microcontrollers adopt high-performance 32-bit ARM® Cortex®-M0+ core and wide voltage operating range MCU. Embed high Up to 32Kbytes flash and 4Kbytes SRAM memory, with a maximum operating frequency of 24MHz. Contains a variety of products with different packaging types. chipset Into multiple channels of I2C, SPI, USART and other communication peripherals, 1 channel of 12bit ADC, 5 channels of 16bit timers, and 2 channels of comparators.

The operating temperature range of the PY32F003 series microcontroller is -40ÿ~85ÿ, and the operating voltage range is 1.7V~5.5V. The chip provides sleep and stop low-power working mode, which can meet different low-power applications.

The PY32F003 series microcontrollers are suitable for a variety of application scenarios, such as controllers, handheld devices, PC peripherals, games and GPS platforms, industrial Industrial applications, etc.

Table 2-1 PY32F003 series product planning and features

peripherals		**PY32F003WxxS**	
		Wx6	wx8
Flash memory (Kbyte)		32	64
SRAM (Kbyte)		4	8
timer	Advanced timer	1 (16-bit)	
	Universal timer	4 (16-bit)	
	Low power timer	1	
	SysTick	1	
	Watchdog	2	
Communication port	SPI	1	
	I2C	1	
	USART	2	
DMA		3ch	
RTC		Yes	
Common port		14	
ADC channel number (External + Internal)		10+2	
Comparator		2	
Maximum Main		32MHz	
Frequency		1.7~5.5V	
Operating Voltage Package		SOP16	

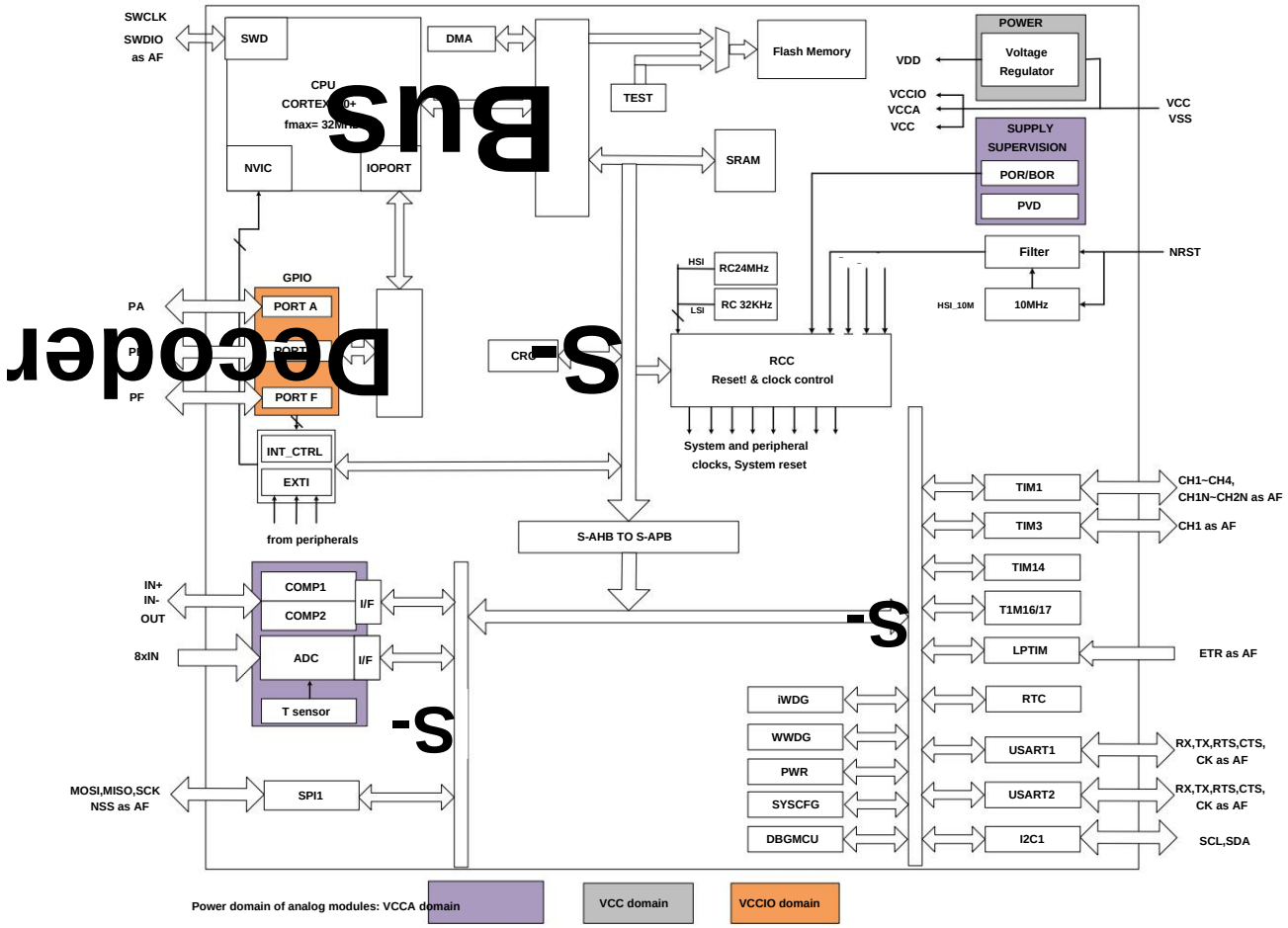


Figure 2-1 Function module

3. Function overview

3.1. Arm® Cortex®-M0+ core

Arm® Cortex®- M0+ is an entry-level 32-bit Arm Cortex processor designed for a wide range of embedded applications. It provides developers with Provides significant benefits, including:

ÿ Simple structure, easy to learn and program

ÿ Ultra-low power consumption, energy-saving operation

ÿ Streamlined code density, etc.

The Cortex-M0+ processor is a 32-bit core with high area and power consumption optimization, and is a 2-level von Neumann architecture. The processor is streamlined but powerful A large instruction set and extensively optimized design provide high-end processing hardware, including single-cycle multipliers, providing the excellence expected from computers with 32-bit architectures performance and higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC).

3.2. Memory

On-chip integrated SRAM. SRAM can be accessed through bytes (8bits), half-word (16bits) or word (32bits).

The integrated Flash on the chip consists of two different physical areas:

ÿ Main flash area, which contains application and user data

ÿ Information area, 4KBytes, which includes the following parts:

- ÿ Option bytes
- ÿ UID bytes
- ÿ System memory

The protection of Flash main memory includes the following mechanisms: ÿ read protection (RDP) to prevent external access. ÿ wrtie protection (WRP) control to prevent unwanted write operations (due to cluttering of the program memory pointer PC). write protect

The minimum protection unit is 4Kbytes.

ÿ Option byte write protection, special unlocking design.

3.3. Clock system

After the CPU is started, the default system clock frequency is HSI 8MHz. The system clock frequency and system clock source can be reconfigured after the program is run. Can The high frequency clocks to choose from are:

ÿ A 4/8/16/22.12/24MHz configurable internal high-precision HSI clock.

ÿ A 32.768KHz configurable internal LSI clock.

ÿ 4~32MHz HSE clock, and can enable CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, HSI frequency is configured by software. At the same time, the CPU NMI interrupt is generated.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. AHB and APB clock frequencies are up to 32MHz.

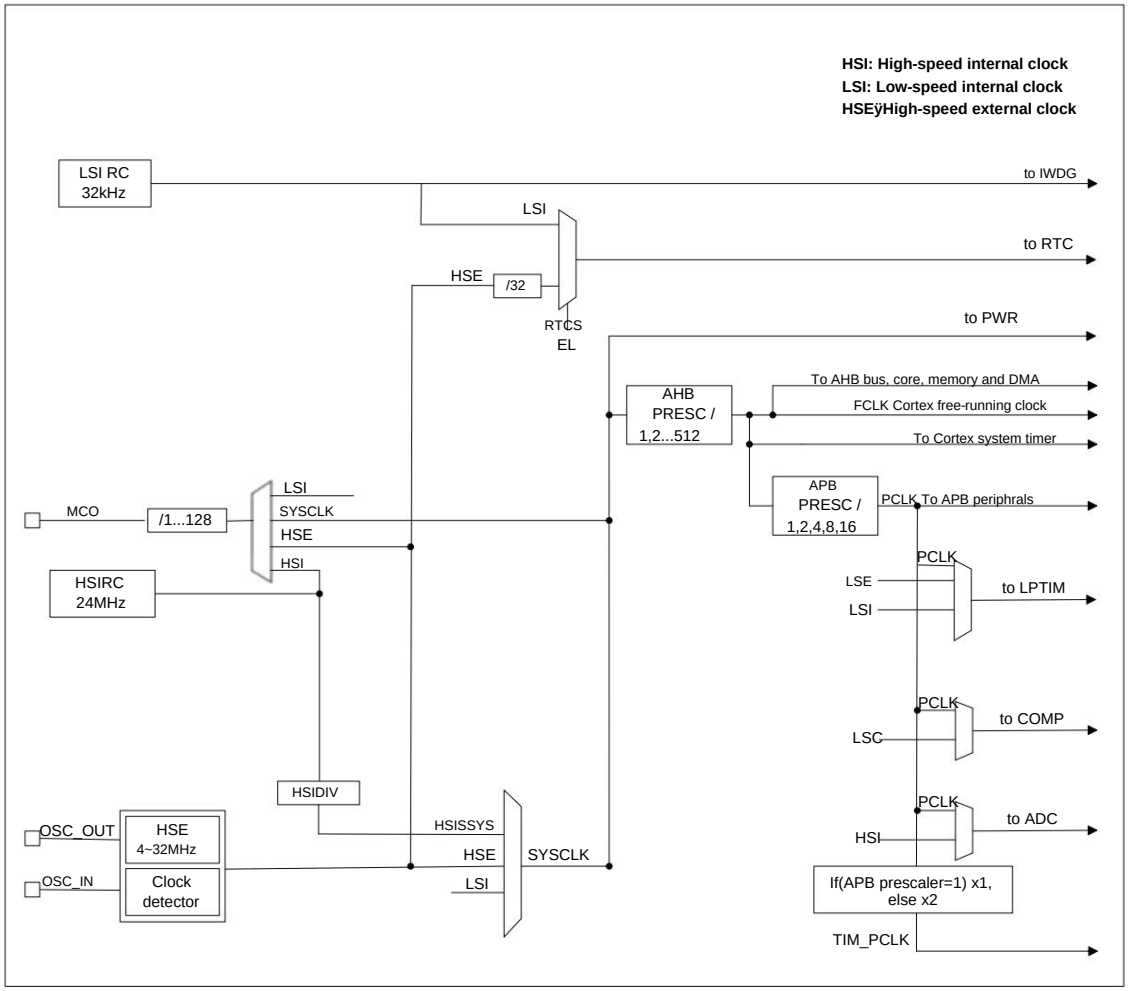


Figure 3-1 System clock structure diagram

3.4.Power management

3.4.1.Power supply block diagram

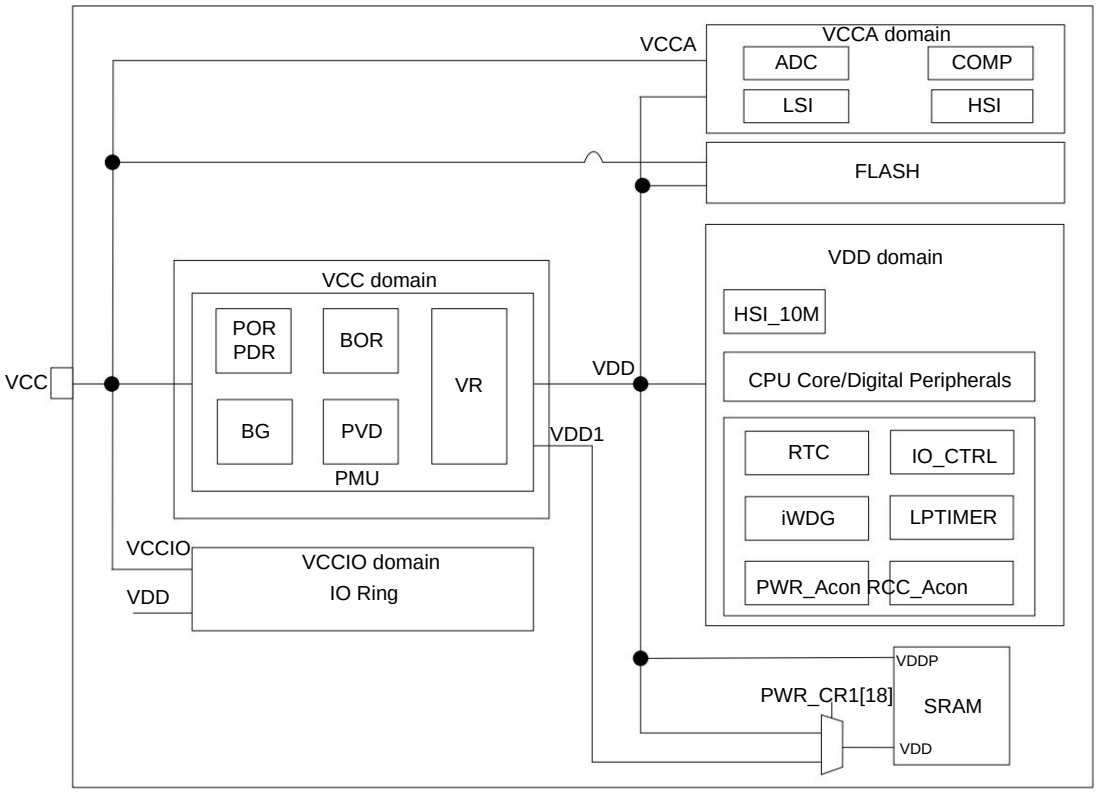


Figure 3-2 Power supply block diagram

Table 3-1 Power supply block diagram

Number power supply		Power value	describe
1	VCC	1.7v~5.5v	Power is provided to the chip through the power pin, and its power supply module is: part of the analog power supply road.
2	VCCA	1.7v~5.5v	Powers most analog modules from VCC PAD (can also be designed separately power pad).
3	VCCIO	1.7v~5.5v	Power IO from VCC PAD
4	VDD	1.2v/1.0v±10%	The output from VR supplies the main logic circuits and SRAM inside the chip. electricity. When MR is powered, it outputs 1.2v. When entering stop mode, according to Software configuration, can be powered by MR or LPR, and determined according to software configuration The LPR output is determined to be 1.2v or 1.0v.

3.4.2.Power supply monitoring

3.4.2.1. Power on and off reset (POR/PDR)

A Power on reset (POR)/Power down reset (PDR) module is designed in the chip to provide power on and power off reset for the chip. The module The block keeps working in all modes.

3.4.2.2. Brown-out reset (BOR)

In addition to POR/PDR, BOR (brown out reset) is also implemented. BOR can only be enabled and disabled through option byte. operate.

When BOR is turned on, the BOR threshold can be selected through the Option byte, and both rising and falling detection points can be configured individually.

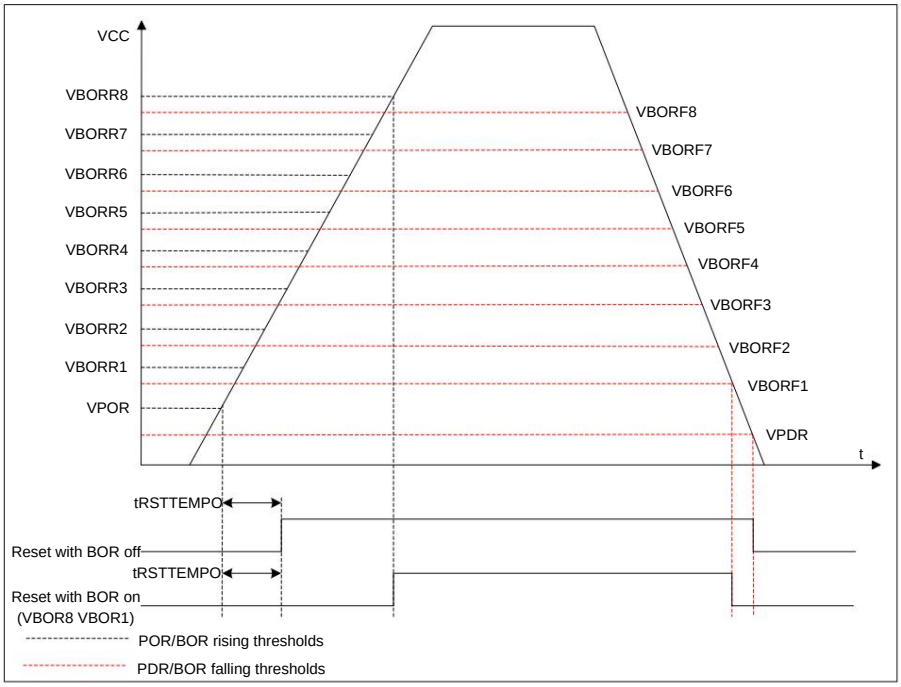


Figure 3-3 POR/PDR/BOR threshold

3.4.2.3.Voltage detection (PVD)

The Programmable Voltage detector (PVD) module can be used to detect the VCC power supply, and the detection points can be configured through registers. when When VCC is higher or lower than the PVD detection point, a corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when VCC rises beyond the detection of PVD point, or VCC drops below the detection point of PVD, an interrupt is generated, and the user can perform emergency shutdown tasks in the interrupt service routine.

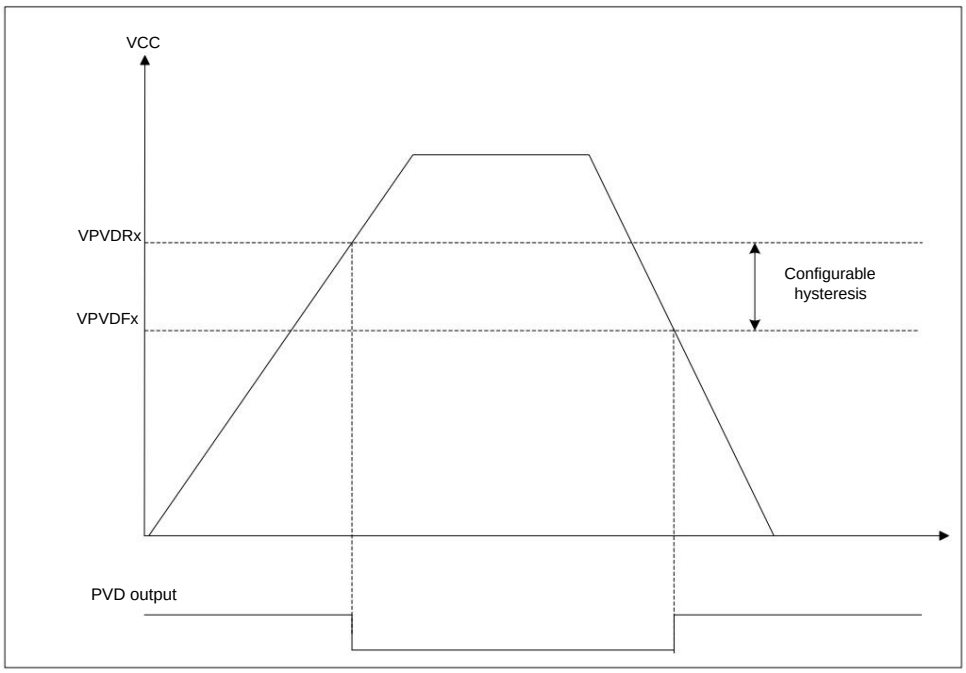


Figure 3-4 PVD threshold

3.4.3.Voltage regulator

The chip is designed with two voltage regulators:

ÿ MR (Main regulator) keeps working when the chip is in normal operation.

ÿ LPR (low power regulator) provides lower power consumption options in stop mode.

3.4.4. Low power consumption mode

In addition to the normal operating mode, the chip has 2 low-power modes:

ÿ **Sleep** mode: The CPU clock is turned off (NVIC, SysTick, etc. work), and peripherals can be configured to keep working. (It is recommended to only enable Modules that must work, close the module after the module work is completed)

ÿ **Stop** mode: In this mode, the contents of SRAM and registers are maintained, HSI is turned off, and the clocks of most modules in the VDD domain are stopped. Lose. GPIO, PVD, COMP output, RTC and LPTIM can wake up from stop mode.

3.5.Reset _

There are two resets designed in the chip: power reset and system reset.

3.5.1.Power reset

A power reset occurs under the following circumstances:

ÿ Power on and off reset (POR/PDR)

ÿ Brown-out reset (BOR)

3.5.2. System reset

A system reset occurs when the following events occur:

ÿ Reset of NRST pin ÿ Window watchdog reset (WWDG) ÿ Independent watchdog reset (IWDG)

ÿ SYSRESETREQ software reset

ÿ option byte load reset (OBL)

ÿ Power reset (POR/PDR, BOR)

3.6.General purpose input and output GPIO

Each GPIO can be configured by software as output (push-pull or open drain), input (floating, pull-up/down, analog), peripheral multiplexing function, and the locking mechanism will freeze the I/O port configuration function.

3.7.DMA

Direct memory access (DMA) is used to provide high-speed data transfer between peripherals and memory or between memory and memory.

The DMA controller has 3 DMA channels, each channel is responsible for managing memory access requests from one or more peripherals. DMA control The arbiter includes an arbiter for handling DMA requests and is used to handle the priority of each DMA request.

DMA supports round-robin buffer management, eliminating the need for user code to intervene when the controller reaches the end of the buffer.

Each channel is directly connected to a dedicated hardware DMA request, and each channel also supports software triggering. These functions are configured through software.

DMA is available for major peripherals: SPI, I2C, USART, all TIMx timers (except TIM14 and LPTIM) and ADC.

3.8. Interruption

PY32F003 is handled by the Cortex-M0+ processor's embedded vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI)
abnormal.

3.8.1. Interrupt controller **NVIC**

NVIC is a tightly coupled IP within the Cortex-M0+ processor. NVIC can handle NMI (non-maskable interrupt) and
Mask external interrupts and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between interrupt events and the initiation of the corresponding interrupt service routine (ISR). ISR vector
Listed in a vector table, stored at a base address of the NVIC. The vector address of the ISR to be executed is determined by the vector table base address and used as an offset
ISR sequence number.

If a high-priority interrupt event occurs and a low-priority interrupt event is waiting for a response, the high-priority interrupt event that arrives later will
will be responded to first. Another type of optimization is called tail-chaining. When returning from a high-priority ISR, then start a pending
A low-priority ISR will skip unnecessary push and pop of processor context. This reduces latency and improves power efficiency.

NVIC features:

ÿ Low-latency interrupt processing

ÿ 4 levels of interrupt priority

ÿ Support 1 NMI interrupt

ÿ Supports 32 maskable external interrupts

ÿ Supports 10 Cortex-M0+ exceptions

ÿ High-priority interrupts can interrupt low-priority interrupt responses

ÿ Support tail-chaining optimization

ÿ Hardware interrupt vector retrieval

3.8.2. Extended interrupt **EXTI**

EXTI adds flexibility in handling physical line events and generates wake-up events when the processor wakes up from stop mode.

EXTI controller has multiple channels including up to 16 GPIOs, 1 PVD output, 2 COMP outputs, as well as RTC and LPTIM
Wake-up signal. Among them, GPIO, PVD and COMP can be configured to trigger rising edge, falling edge or double edge. Any GPIO signal is configured by selecting the signal
Set to EXTI0~15 channels.

Each EXTI line can be independently masked via registers.

The EXTI controller can capture pulses shorter than the internal clock period.

Registers in the EXTI controller latch each event so that the processor can recognize wake-ups after waking up from stop mode, even in stop mode.
source, or identify the GPIO and event that caused the interrupt.

3.9.**Analog** -to-digital converter **ADC**

The chip has a 12-bit SARADC. The module has up to 5 channels to be measured, including 3 external channels and 2 internal channels.
road.

The conversion mode of each channel can be set to single, continuous, scan, and discontinuous modes. Conversion results are stored in left-aligned or right-aligned 16-bit
in the data register.

Analog watchdogs allow applications to detect if the input voltage exceeds user-defined high or low thresholds.

The ADC operates at low frequency and achieves very low power consumption.

At the end of sampling, the end of conversion, the end of continuous conversion, and when the conversion voltage exceeds the threshold during the analog watchdog, an interrupt request is generated.

3.10.Timer _

The characteristics of different timers of PY32F003 are shown in the following table:

Table 3-2 Timer characteristics

type	**Timer**	Bit width count direction prescaler **DMA** capture/compare channe	complementary output	
Advanced timer TIM1		16 bit	superior, Down, Center aligned	1~65536 supported	4	3
Universal timer	TIM3	16-bit	superior, Down, Center aligned	1~65536 supported	4	-
	TIM14	16-bit	Go	1~65536 -	1	-
	TIM16,TIM17 16-bit		up, go up	1~65536 support	1	1

3.10.1. Advanced timer

The advanced timer (TIM1) consists of a 16-bit autoload counter driven by a programmable divider. It can be used in various scenarios, including Includes: pulse length measurement of input signals (input capture), or generation of output waveforms (output compare, output PWM, complementary with dead zone insertion) PWM).

TIM1 consists of 4 independent channels used for:

ÿ Input capture

ÿ Output comparison

ÿ PWM generation (edge or center aligned mode)

ÿ Single pulse mode output

If TIM1 is configured as a standard 16-bit timer, it has the same characteristics as the TIMx timer. Occurs if configured for 16-bit PWM device, it has full modulation capability (0-100%).

In MCU debug mode, TIM1 can freeze counting.

Timer features with the same architecture are shared, so TIM1 can work with other timers via the timer linking feature for synchronization or event link.

TIM1 supports DMA function.

3.10.2. General timer

3.10.2.1.TIM3

The TIM3 general-purpose timer is composed of a 16-bit auto-reload counter driven by a 16-bit programmable divider. Has 4 independent channels, each Used for input capture/output comparison, PWM or single pulse mode output.

TIM3 can work with TIM1 through the timer link function.

TIM3 supports DMA function.

TIM3 is capable of processing quadrature (incremental) encoder signals and digital outputs from 1 to 3 Hall effect sensors.

In MCU debug mode, TIM3 can freeze counting.

3.10.2.2.TIM14

The general-purpose timer TIM14 consists of a 16-bit autoload counter driven by a programmable prescaler.

TIM14 has 1 independent channel for input capture/output comparison, PWM or single pulse mode output.

In MCU debug mode, TIM14 can freeze counting.

3.10.2.3.TIM16/TIM17

TIM16 and TIM17 consist of a 16-bit autoload counter driven by a programmable prescaler.

TIM16/TIM17 has 1 independent channel for input capture/output comparison, PWM or single pulse mode output.

TIM16/TIM17 have complementary outputs with dead band.

TIM16/TIM17 supports DMA function.

In MCU debug mode, TIM16/TIM17 can freeze counting.

3.10.3. Low power timer

LPTIM is a 16-bit up counter and contains a 3-bit prescaler. Only single counting is supported.

LPTIM can be configured as stop mode wake-up source.

In MCU debug mode, LPTIM can freeze the count value.

3.10.4.IWDG

An Independent watchdog (IWDG for short) is integrated into the chip. This module has high security level, accurate timing and flexible use.
specialty. IWDG detects and resolves functional confusion caused by software failures and triggers a system reset when the counter reaches a specified timeout value.

IWDG is clocked by LSI, so it can keep working even if the main clock fails.

IWDG is best suited for applications that require watchdog as an independent process from the main application and do not have high timing accuracy constraints.

Through the control of option byte, IWDG hardware mode can be enabled.

IWDG is the wake-up source of stop mode and wakes up stop mode by reset.

In MCU debug mode, IWDG can freeze the count value.

3.10.5. WWDG

The system window watchdog is based on a 7-bit downstream counter and can be set to free-running. When a problem arises, it can serve as a look
Watchdog to reset the system. The counting clock is the APB clock (PCLK). It has early warning interrupt capability, and the counter can be frozen in MCU debug mode
Knot.

3.10.6. SysTick timer

The SysTick counter is designed for use with real-time operating systems (RTOS), but can also be used as a standard down counter.

SysTick features:

ÿ 24bit count down

ÿ Self-loading capability

ÿ When the counter reaches 0, an interrupt can be generated (can be masked)

3.11.Real -time clock RTC

The real-time clock is an independent timer. The RTC module has a set of continuous counting counters. Under the corresponding software configuration, it can provide the clock date.
calendar function. Modifying the counter value can reset the current time and date of the system.

RTC is a 32-bit programmable counter with a prescaler coefficient up to 220 .

The RTC counter clock source can be LSI and can be used as a stop wake-up source.

RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).

RTC supports clock calibration.

In MCU debug mode, RTC can freeze counting.

3.12. I2C interface

The I2C (inter-integrated circuit) bus interface connects the microcontroller and the serial I2C bus. It provides multi-master functionality, controlling all I2C master Line-specific sequencing, protocols, arbitration, and timing. Supports standard (Sm) and fast (Fm).

I2C features:

ÿ Slave and master mode

ÿ Multi-host function: you can be a master or a slave

ÿ Support different communication speeds

- ÿ Standard mode (Sm): up to 100kHz
- ÿ Fast mode (Fm): up to 400kHz

ÿ As Master

- ÿ Generate Clock
- ÿ Generation of Start and Stop

ÿ as slave

- ÿ Programmable I2C address detection
- ÿ Discovery of Stop bit

ÿ 7-bit addressing mode

ÿ General call

ÿ Status flag bit

- ÿ Transmit/receive mode flag bit
- ÿ Byte transfer completion flag bit
- ÿ I2C busy flag bit

ÿ Error flag bit

- ÿ Master arbitration loss
- ÿ ACK failure after address/data transmission
- ÿ Start/Stop error ÿ Overrun/
  Underrun (clock stretching function disabled)

ÿ Optional clock stretching function

ÿ Single-byte buffer with DMA capability

ÿ Software reset

ÿ Analog noise filtering function

3.13.Universal synchronous asynchronous receiver-transmitter USART

The Universal Synchronous Asynchronous Receiver-Transmitter (USART) provides a flexible method to communicate with external devices using the industry standard NRZ asynchronous serial data format.

Full-duplex data exchange between them. USART utilizes a fractional baud rate generator to provide a wide range of baud rate selections.

It supports synchronous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Supports automatic baud rate detection.

High-speed data communication can be achieved using the DMA mode with multiple buffer configurations.

USART features:

ÿ Full-duplex asynchronous communication

ÿ NRZ standard format

ÿ Configurable 16x or 8x oversampling, increasing flexibility in speed and clock tolerance

ÿ Programmable baud rate shared by sending and receiving, up to 4.5Mbit/s

ÿ Automatic baud rate detection

ÿ Programmable data length 8 or 9 bits

ÿ Configurable stop bits (1 or 2 bits)

ÿ Synchronous mode and clock output function for synchronous communication

ÿ Single-wire half-duplex communication

ÿ Independent transmit and receive enable bits

ÿ Hardware flow control

ÿ Receive/send bytes via DMA buffer

ÿ Inspection mark

- ÿ The receiving buffer is full
- ÿ Send buffer empty
- ÿTransmission ends

ÿ Parity Control

- ÿ Send check digit
- ÿ Verify the received data

ÿ Flagged interrupt sources

- ÿ CTS changes
- ÿ The sending register is empty
- ÿSending completed
- ÿ The receiving data register is full
- ÿ Bus idle detected
- ÿ Overflow error
- ÿ Frame error
- ÿ Noisy operation
- ÿ Detect errors

ÿ Multi-processor communication

- ÿ If the addresses do not match, enter silent mode

ÿ Wake up from silent mode: through idle detection and address flag detection

3.14. Serial Peripheral Interface **SPI**

The Serial Peripheral Interface (SPI) allows the chip to communicate with external devices in a half-duplex, full-duplex, or simplex synchronous serial manner. This interface can be configured into master mode and provides communication clock (SCK) to external slave devices. The interface can also work in a multi-master configuration.

SPI characteristics are as follows:

ÿ Master or slave mode

ÿ 3-wire full-duplex synchronous transmission

ÿ 2-wire half-duplex synchronous transmission (with bidirectional data line)

ÿ 2-wire simplex synchronous transmission (no bidirectional data line)

ÿ 8-bit or 16-bit transmission frame selection

ÿ Support multi-master mode

ÿ 8 master mode baud rate prescaler coefficients (maximum fPCLK/4)

ÿ Slave mode frequency (maximum fPCLK/4)

ÿ NSS management can be performed by software or hardware in both master mode and slave mode: dynamic change of master/slave operating mode

ÿ Programmable clock polarity and phase

ÿ Programmable data order, MSB first or LSB first

ÿ Dedicated send and receive flags that trigger interrupts

ÿ SPI bus busy status flag

ÿ Motorola Mode

ÿ Main mode faults and overloads that can cause interruptions

ÿ 2 32bit Rx and Tx FIFOs with DMA capability

3.15. SWD

The ARM SWD interface allows serial debugging tools to be connected to the PY32F003.

4.Pin configuration

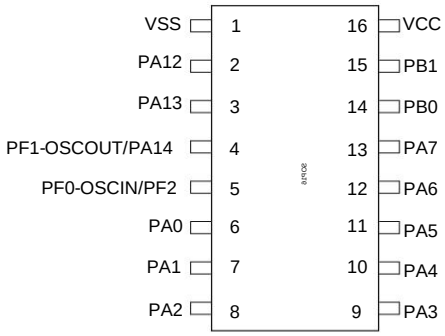


Figure 4-1 SOP16 Pinout1 PY32F003W1XS

Table 4-1 Terms and symbols for pin definitions

type		symbol	definition
port type		S	Supply pin
		G	Ground pin
		I/O	Input/output pin
		NC	no definition
Port structure		COM	normal 5V port, supports analog input and output functions
		RST	reset port, with internal weak pull-up resistor, does not support analog input and output functions
Notes			Unless otherwise noted, all ports are left as floating inputs between and after reset.
Port function	Additional		Function selected via GPIOx_AFR register
	functions for reuse		Functions directly selected or enabled through peripheral registers

Table 4-2 SOP16 pin definition

Package type	reset	I/O	I/O structure	Notes	Port function	
SOP16					Reuse function	Additional features
1	VSS	S			Ground	
2	PA12	I/O	COM		SPI1_MOSI USART1_RTS TIM1_ETR USART2_RTS EVENTOUT I2C_SDA COMP2_OUT	-
3	PA13(SWDIO)	I/O	COM	(2)	SWDIO IR_OUT EVENTOUT	-

					SPI1_MISO	
					TIM1_CH2	
					USART1_RX	
					MCO	
4	PF1-OSC_OUT-(PF1)	I/O	COM	(3)	USART2_TX	OSC_OUT
					USART1_TX	
					USART2_RX	
					I2C_SCL	
					SP1_NSS	
					TIM14_CH	
	PA14(SWCLK)	I/O	COM	(2)(3)	SWCLK	-
					USART1_TX	
					USART2_TX	
					EVENTOUT	
					MCO	
5	PF0-OSC_IN-(PF0)	I/O	COM	(3)	USART2_RX	OSC_IN
					TIM14_CH1	
					USART1_RX	
					USART2_TX	
					I2C_SDA	
	PF2-NRST	I/O	RST	(1)(3)	MCO	NRST
					USART2_RX	
6	PA0	I/O	COM		USART1_CTS	ADC_IN0 COMP1_INM
					USART2_CTS	
					COMP1_OUT	
					TIM1_CH3	
					TIM1_CH1N	
					SPI1_MISO	
					USART2_TX	
					IR_OUT	
7	PA1	I/O	COM		SPI1_SCK	COMP1_INP ADC_IN1
					USART1_RTS	
					USART2_RTS	
					EVENTOUT	
					SPI1_MOSI	
					USART2_RX	
					TIM1_CH4	
					TIM1_CH2N	
					MCO	
8	PA2	I/O	COM		SPI1_MOSI	COMP2_INM ADC_IN2
					USART1_TX	
					USART2_TX	
					COMP2_OUT	
					SPI1_SCK	
					TIM3_CH1	

					I2C_SDA	
9	PA3	I/O	COM		USART1_RX USART2_RX EVENTOUT SPI1_MOSI TIM1_CH1 I2C_SCL	COMP2_INP ADC_IN3
10	PA4	I/O	COM		SPI1_NSS USART1_CK TIM14_CH1 USART2_CK ENENTOUT RTC_OUT TIM3_CH3 USART2_TX	ADC_IN4
11	PA5	I/O	COM		SPI1_SCK LPTIM_ETR EVENTOUT TIM3_CH2 USART2_RX MCO	ADC_IN5
12	PA6	I/O	COM		SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 EVENTOUT COMP1_OUT USART1_CK RTC_OUT	ADC_IN6
13	PA7	I/O	COM		SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM14_CH1 TIM17_CH1 EVENTOUT COMP2_OUT USART1_TX USART2_TX I2C_SDA SPI1_MISO	ADC_IN7
14	PB0	I/O	COM		SPI1_NSS TIM3_CH3 TIM1_CH2N EVENTOUT COMP1_OUT	ADC_IN8

15	PB1	I/O	COM		TIM14_CH1 TIM3_CH4 TIM1_CH3N EVENTOUT	COMP1_INM ADC_IN9
16	VCC	S			Digital power supply	

Note:

(1) Selecting PF2 or NRST is configured through option bytes.

(2) After reset, the two pins PA13 and PA14 are configured as SWDIO and SWCLK AF functions. The former has an internal pull-up resistor and the latter has an internal pull-up resistor. pull resistor is activated.

(3) The two IO ports are connected to the same pin. Only one of the IO ports can be used at the same time, and the other IO must be configured as Simulation mode (MODEy[1:0] is 0B11).

4.1.Port A multiplexing function mapping

Table 4-3 Port A multiplexing function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART1_CTS	-		USART2_CTS	-	-	COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	USART2_TX	SPI1_MISO	-	-	TIM1_CH3	TIM1_CH1N	IR_OUT
PA1	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_SCK	USART1_RTS	-		USART2_RTS	-	-	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	USART2_RX	SPI1_MOSI	-	-	TIM1_CH4	TIM1_CH2N	MCO
PA2	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MOSI	USART1_TX	-		USART2_TX	-	-	COMP2_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	-	SPI1_SCK	-	I2C_SDA	TIM3_CH1	-	-
PA3	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		USART1_RX	-		USART2_RX	-	-	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	-	SPI1_MOSI	-	I2C_SCL	TIM1_CH1	-	-
PA4	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_NSS	USART1_CK			TIM14_CH1	USART2_CK	-	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	USART2_TX	-	-	-	TIM3_CH3	-	RTC_OUT
PA5	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_SCK	-	-		-	LPTIM1_ETR	-	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	-	USART2_RX	-	-	-	TIM3_CH2	-	MCO
PA6	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MISO	TIM3_CH1	TIM1_BKIN		-	TIM16_CH1	-	COMP1_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	USART1_CK	-	-	-	-	-	-	RTC_OUT
PA7	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	USART1_TX	USART2_TX	SPI1_MISO	-	I2C_SDA	-	-	-
PA12	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SPI1_MOSI	USART1_RTS	TIM1_ETR	-	USART2_RTS	EVENTOUT	I2C_SDA	COMP2_OUT
PA13	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	USART1_RX	-	SPI1_MISO	-	-	TIM1_CH2	-	MCO
PA14	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7

	SWCLK	USART1_TX	-	-	USART2_TX	-	-	EVENTOUT
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	-	-	-	-	-	-	-	MCO

4.2. Port **B** multiplexing function mapping

Table 4-4 Port B multiplexing function mapping

port	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PB0	SPI1_NSS	TIM3_CH3	TIM1_CH2N	-	-	EVENTOUT	-	COMP1_OUT
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT

4.3. Port **F** multiplexing function mapping

Table 4-5 Port F multiplexing function mapping

port	**AF0**	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PF0-OSC_IN	-	-	TIM14_CH1		USART2_RX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_RX	USART2_TX	-	-	I2C_SDA	-	-	-
	AF0	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PF1_OSC_OUT	-	-	-		USART2_TX	-	-	-
	AF8	**AF9**	**AF10**	**AF11**	**AF12**	**AF13**	**AF14**	**AF15**
	USART1_TX	USART2_RX	SPI1_NSS	-	I2C_SCL	TIM14_CH1	-	-
	AF0	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**	**AF6**	**AF7**
PF2-NRST	-	-	-		USART2_RX	-	MCO	-

5. Memory mapping

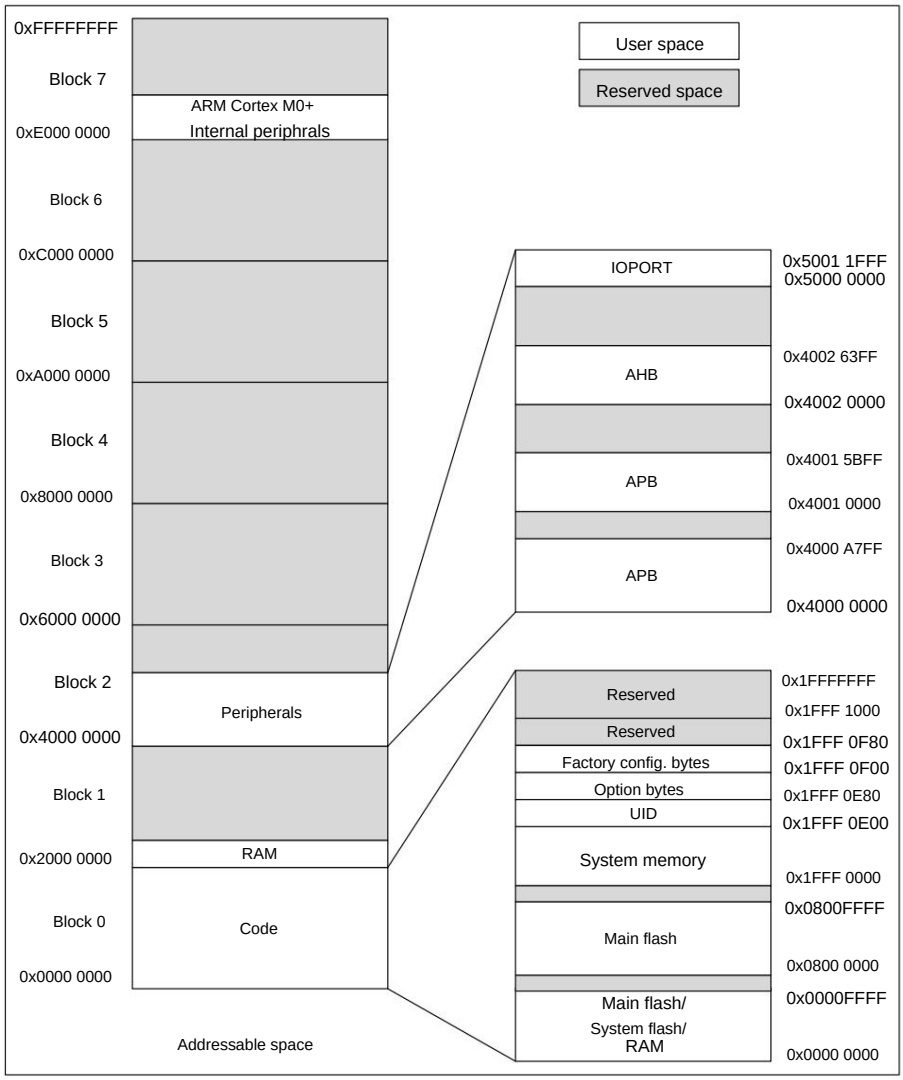


Figure 5-1 Memory map

Table 5-1 Memory address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 2000-0x3FFF FFFF 512MBytes Reserved			
	0x2000 0000-0x2000 1FFF 8KBytes SRAM			Depending on the hardware, the maximum SRAM is 8kBytes
Code	0x1FFF 1000-0x1FFF FFFF 4KBytes		Reserved	
	0x1FFF 0F80-0x1FFF 0FFF 128Bytes		Reserved	
	0x1FFF 0F00-0x1FFF 0F7F 128Bytes		Factory config	Store HSI triming data, flash erase time configuration
	0x1FFF 0E80-0x1FFF 0EFF 128Bytes Option bytes 0x1FFF			parameter option bytes
	0E00-0x1FFF 0E7F 128Bytes UID 0x1FFF			Unique ID
	0000-0x1FFF 0DFF 3.5KBytes System memory 0x0801 0000-0x1FFF			stores boot loader
	FFFF 384MBytes Reserved 0x0800 0000-0x0800 FFFF			
	64KBytes Main flash memory 0x0001 0000-0x07FF FFFF 8MBytes			
	Reserved			

	0x0000 0000-0x0000 FFFF 64KBytes		Select according to Boot configuration: 1) Main flash memory 2) System memory 3) SRAM	

Note:

Except for 0x1FFF 0E00-0x1FFF 0E7F, the above spaces are marked as reserved spaces, which cannot be written, read as 0, and generate response error.

Table 5-2 Peripheral register addresses

Bus	Boundary Address	Size	Peripheral
	0xE000 0000-0xE00F FFFF 1Mbytes	0x5000	M0+
IOPORT	1800-0x5FFF FFFF 256MBytes	0x5000 1400-0x5000	Reserved(1)
	17FF 1KBytes	0x5000 1000-0x5000 13FF	GPIOF
	1KBytes	0x5000 0C00-0x5000 0FFF 1Kbytes	Reserved
	0x5000 0800-0x5000 0BFF 1Kbytes	0x5000	Reserved
	0400-0x5000 07FF 1Kbytes	0x5000	Reserved
	0000-0x5000 03FF 1Kbytes	0x4002	GPIOB
	3400-0x4FFFFFFF		GPIOA
AHB			Reserved
	0x4002 300C-0x4002 33FF	1Kbytes	Reserved
	0x4002 3000-0x4002 3008		CRC
	0x4002 2400-0x4002 2FFF		Reserved
	0x4002 2124-0x4002 23FF	1KBytes	Reserved
	0x4002 2000-0x4002 2120		Flash
	0x4002 1C00-0x4002 1FFF 3KBytes	0x4002	Reserved
	1888-0x4002 1BFF	1Kbytes	Reserved
	0x4002 1800-0x4002 1884		EXTI(2)
	0x4002 1400-0x4002 17FF 1Kbytes	0x4002	Reserved
	1064-0x4002 13FF	1KBytes	Reserved
	0x4002 1000-0x4002 1060		RCC(2)
	0x4002 0C00-0x4002 0FFF 1KBytes	0x4002	Reserved
	0040-0x4002 03FF	1KBytes	Reserved
	0x4002 0000-0x4002 003C		DMA
APB	0x4001 5C00-0x4001 FFFF 32KBytes	0x4001	Reserved
	5880-0x4001 5BFF	1KBytes	Reserved
	0x4001 5800-0x4001 587F		DBG
	0x4001 4C00-0x4001 57FF 3KBytes	0x4001	Reserved
	4850-0x4001 4BFF	1KBytes	Reserved
	0x4001 4800-0x4001 484C		TIM17
	0x4001 4450-0x4001 47FF	1KBytes	Reserved
	0x4001 4400-0x4001 404C		TIM16
	0x4001 3C00-0x4001 43FF 2KBytes	0x4001	Reserved
	381C-0x4001 3BFF	1KBytes	Reserved
	0x4001 3800-0x4001 3018		USART1
	0x4001 3400-0x4001 37FF 1Kbytes	0x4001	Reserved
	3010-0x4001 33FF	1Kbytes	Reserved
	0x4001 3000-0x4001 300C		SPI1
	0x4001 2C50-0x4001 2FFF 1Kbytes		Reserved

	0x4001 2C00-0x4001 2C4C		TIM1
	0x4001 2800-0x4001 2BFF	1Kbytes	Reserved
	0x4001 270C-0x4001 27FF	1Kbytes	Reserved
	0x4001 2400-0x4001 2708		ADC
	0x4001 0400-0x4001 23FF	8Kbytes	Reserved
	0x4001 0220-0x4001 03FF	1KBytes	Reserved
	0x4001 0200-0x4001 021F		COMP1 and COMP2
	0x4001 0000-0x4001 01FF		SYSCFG
	0x4000 B400-0x4000 FFFF	19KBytes	Reserved
	0x4000 B000-0x4000 B3FF	1KBytes	Reserved
	0x4000 8400-0x4000 AFFF	11KBytes	Reserved
	0x4000 8000-0x4000 83FF	1KBytes	Reserved
	0x4000 7C28- 0x40007FFF	1KBytes	Reserved
	0x4000 7C00-0x4000 7C24		LPTIM
	0x4000 7400-0x4000 7BFF	2KBytes	Reserved
	0x4000 7018-0x4000 73FF	1KBytes	Reserved
	0x4000 7000-0x4000 7014		PWR(3)
	0x4000 5800-0x4000 6FFF	6KBytes	Reserved
	0x4000 5434-0x4000 57FF	1KBytes	Reserved
	0x4000 5400-0x4000 5430		I2C
	0x4000 4800-0x4000 53FF	3KBytes	Reserved
	0x4000 441C-0x4000 47FF	1KBytes	Reserved
	0x4000 4400-0x4000 4418		Reserved
	0x4000 3C00-0x4000 43FF	1KBytes	Reserved
	0x4000 3800-0x4000 3BFF	1KBytes	Reserved
	0x4000 3400-0x4000 37FF	1KBytes	Reserved
	0x4000 3014-0x4000 33FF	1KBytes	Reserved
	0x4000 3000-0x4000 0010		iWDG
	0x4000 2C0C-0x4000 2FFF	1KBytes	Reserved
	0x4000 2C00-0x4000 2C08		WWDG
	0x4000 2830-0x4000 2BFF	1KBytes	Reserved
	0x4000 2800-0x4000 282C		RTC(3)
	0x4000 2400-0x4000 27FF	1KBytes	Reserved
	0x4000 2054-0x4000 23FF	1KBytes	Reserved
	0x4000 2000-0x4000 0050		TIM14
	0x4000 1800-0x4000 1FFF	2KBytes	Reserved
	0x4000 1400-0x4000 17FF	1KBytes	Reserved
	0x4000 1000-0x4000 13FF	1KBytes	Reserved
	0x4000 0800-0x4000 0FFF	2KBytes	Reserved
	0x4000 04 50-0x4000 07FF	1Kbytes	Reserved
	0x4000 0400-0x4000 044C		TIM3
	0x4000 0000-0x4000 03FF	1KBytes	Reserved

Note:

(1) The address space marked as Reserved in AHB in the above table cannot be written, the readback is 0, and a hardfault occurs; APB is marked as The Reserved address space cannot be written, and is read back as 0, so no hardfault will occur.

(2) Not only supports 32bit word access, but also supports halfword and byte access.

(3) Not only supports 32bit word access, but also supports halfword access.

6. Electrical characteristics

6.1.Test conditions

Unless otherwise stated, all voltages are referenced to VSS.

6.1.1. Minimum and maximum values

Unless otherwise specified, through the chip mass production test screening at the ambient temperature TA=25°C and TA=TA(max), it is guaranteed to be stable under the worst ambient temperature.
The minimum and maximum values are reached depending on the temperature, supply voltage and clock frequency.

Data based on electrical property results, design simulations, and/or process parameters annotated below the table and not tested in production. Minimum and maximum values
Referring to sample testing, take the average plus or minus three times the standard deviation.

6.1.2.Typical values

Unless otherwise stated, typical data is based on TA=25°C and VCC=3.3V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch and testing over all temperature ranges. 95% of the chip errors are less than or equal to
to the given value.

6.2.Absolute maximum ratings

If applied to the chip in excess of the absolute maximum values given in the table below, it may cause permanent damage to the chip. Here is just a list of what we can afford
The intensity rating does not mean that the device will function correctly under these conditions. Working under maximum conditions for a long time may affect the reliability of the chip.
sex.

Table 6-1 Voltage characteristics (1)

symbol		minimum value	maximum value	unit
VCC	Description of the input	-0.3	6.25	V
VIN	voltage of other pins of the external	-0.3	VCC+0.3	V

main power supply (1) The power VCC and ground VSS pins must always be connected to the external power supply system within the allowed range.

Table 6-2 Current characteristics

symbol	Describe	Maximum value	unit
IVCC	the total current flowing into the VCC pin (supply current) (1)	100	mA
IVSS	The total current flowing out of the VSS pin (outgoing current) (1)	100	
IIO(PIN)	The output of COM IO sinks current	20	
	and all IO sources current	-20	

(1) The power supply VCC and ground VSS pins must always be connected to the external power supply system within the allowed range.

Table 6-3 Temperature characteristics

symbol	describe	numerical value	unit
TSTG storage temperature range		-65~+150	ÿ
TO	operating temperature range	-40~+85	ÿ

6.3. Working conditions

6.3.1.General working conditions

Table 6-4 General working conditions

symbol	parameter	condition	Minimum value	Maximum value	unit
htK	Internal AHB clock frequency -		0	32	MHz
fPCLK	Internal APB clock frequency -		0	32	MHz
VCC standard operating voltage		-	1.7	5.5	V
VIN	IO input voltage ambient	-	-0.3	VCC+0.3 V	
TA	temperature junction	-	-40	85	ÿ
TJ	temperature	-	-40	90	ÿ

6.3.2. Power on and off working conditions

Table 6-5 Power-on and power-off working conditions

symbol	parameter	condition	Minimum value	Maximum value	unit
tVCC	VCC rise rate	-	0	ÿ	us/V
	VCC falling rate	-	20	ÿ	

6.3.3. Embedded reset and **LVD** module features

Table 6-6 Embedded reset module characteristics

Symbol		Condition	minimum value	typical value	maximum value	unit
tRSTTEMPO(1)	Parameter reset reset time	-	-	4.0	7.5	ms
VPOR/PDR	POR/PDR reset threshold	Rising edge 1.50 (2)		1.60	1.70	V
		Falling edge 1.45 (1)		1.55	1.65(2)	V
VBOR1	BOR threshold 1	Rising edge 1.70 (2)		1.80	1.90	V
		Falling edge 1.60 Rising		1.70	1.80(2)	V
VBOR2	BOR threshold 2	edge 1.90 (2) Falling edge		2.00	2.10	V
		1.80		1.90	2.00(2)	V
VBOR3	BOR threshold 3	Rising edge 2.10(2)		2.20	2.30	V
		Falling edge 2.00		2.10	2.20(2)	V
VBOR4	BOR threshold 4	Rising edge 2.30(2)		2.40	2.50	V
		Falling edge 2.20 Rising		2.30	2.40(2)	V
VBOR5	BOR threshold 5	edge 2.50 (2) Falling edge		2.60	2.70	V
		2.40 Rising edge 2.70		2.50	2.60(2)	V
VBOR6	BOR threshold 6	(2) Falling edge 2.60		2.80	2.90	V
		Rising edge 2.90 (2)		2.70	2.80(2)	V
VBOR7	BOR threshold 7	Falling edge 2.80 Rising		3.00	3.10	V
		edge 3.10 (2) Falling		2.90	3.00(2)	V
VBOR8	BOR threshold 8	edge 3.00		3.20	3.30	V
				3.10	3.20(2)	V

VPVD0	PVD threshold 0	Rising edge 1.70(2)		1.80	1.90	V
		Falling edge 1.60 Rising		1.70	1.80(2)	V
VPVD1	PVD threshold 1	edge 1.90(2) Falling		2.00	2.10	V
		edge 1.80 Rising edge		1.90	2.00(2)	V
VPVD2	PVD Threshold 2	2.10(2) Falling edge 2.00		2.20	2.30	V
		Rising edge 2.30(2)		2.10	2.20(2)	V
VPVD3	PVD threshold 3	Falling edge 2.20 Rising		2.40	2.50	V
		edge 2.50(2) Falling		2.30	2.40(2)	V
VPVD4	PVD threshold 4	edge 2.40 Rising edge		2.60	2.70	V
		2.70(2) falling edge		2.50	2.60(2)	V
VPVD5	PVD threshold 5	2.60		2.80	2.90	V
				2.70	2.80(2)	V
VPVD6	PVD threshold 6	Rising edge 2.90(2)		3.00	3.10	V
		Falling edge 2.80		2.90	3.00(2)	V
VPVD7	PVD threshold 7	Rising edge 3.10(2)		3.20	3.30	V
		Falling edge 3.00		3.10	3.20(2)	V
VPOR_PDR_hyst(1)	POR/PDR hysteresis voltage	-		50		mV
VPVD_BOR_hyst(1)	PVD hysteresis voltage			100		mV
Idd(PVD)	PVD power consumption			0.6		uA
Idd(BOR)	BOR power consumption			0.6		uA

(1) Guaranteed by design, not tested in production.

(2) The data is based on assessment results and is not tested in production.

6.3.4. Operating current characteristics

Table 6-7 Operating mode current

symbol	condition					Typical value(1)	Maximum value	unit
	system clock	Frequency	code runs	peripheral clock	FLASH sleep			
IDD(run)	HSI	24MHz	While (1)	Flash	ON DISABLE	1.5	-	mA
					OFF DISABLE	0.9	-	
		16MHz			ON DISABLE	1.1	-	
					OFF DISABLE	0.7	-	
		8MHz			ON DISABLE	0.7	-	
					OFF DISABLE	0.5	-	
		4MHz			ON DISABLE	0.5	-	
					OFF DISABLE	0.35	-	
	LSI	32.768kHz			ON DISABLE	170	-	uA
					OFF DISABLE	170	-	
	LSI	32.768kHz			ON ENABLE	95	-	uA
					OFF ENABLE	95	-	

(1) The data is based on assessment results and is not tested in production.

Table 6-8 sleep mode current

symbol	condition				Typical value (1)	Maximum value	unit
	System clock frequency	Peripheral clock		FLASH sleep			
IDD(sleep)	HSI	24MHz	ON	DISABLE	1	-	mA
			OFF	DISABLE	0.6	-	mA
		16MHz	ON	DISABLE	0.75	-	mA
			OFF	DISABLE	0.5	-	mA
		8MHz	ON	DISABLE	0.5	-	mA
			OFF	DISABLE	0.35	-	mA
		4MHz	ON	DISABLE	0.4	-	mA
			OFF	DISABLE	0.35	-	mA
	LSI	32.768kHz	ON	DISABLE	170	-	uA
			OFF	DISABLE	170	-	uA
	LSI	32.768kHz	ON	ENABLE	95	-	uA
			OFF	ENABLE	96	-	uA

(1) The data is based on assessment results and is not tested in production.

Table 6-9 stop mode current

symbol	condition					Typical value (1)	Maximum value	unit
	VCC	VDD	MR/LPR	LSI	Peripheral clock			
IDD(stop)	1.7~5.5V	1.2V	MR	-	-	70	-	uA
		1.2V	LPR	ON	RTC+IWDG+LPTIM	6	-	
					iWDG	6	-	
					LPTIM	6	-	
					RTC	6	-	
				OFF	No	6	-	
		1.0V		ON	RTC+IWDG+LPTIM	4.5	-	
					iWDG	4.5	-	
					LPTIM	4.5	-	
					RTC	4.5	-	
				OFF	No	4.5	-	

(1) The data is based on assessment results and is not tested in production.

6.3.5. Low power mode wake-up time

Table 6-10 Low power mode wake-up time

symbol	Parameter(1)		condition		Typical value (2)	Maximum value	unit
TWUSLEEP	Sleep wake-up time		-		1.65		us
TWUSTOP	Stop When waking up between	MR powered	Execute program in Flash, HSI (24Mhz) operates is the system clock		3.5		us
		LPR power supply	Execute the program in Flash, HSI as system clock	VDD=1.2V	6		us
				VDD=1.0V	6		

(1) The measurement of wake-up time is from the start of wake-up time to the first instruction read by the user program.

(2) The data is based on assessment results and is not tested in production.

6.3.6. External clock source characteristics

6.3.6.1.External high-speed clock

In the bypass mode of HSE (the HSEBYP of RCC_CR is set), the high-speed oscillator circuit in the chip stops working, and the corresponding IO is used as a standard Correct GPIO usage.

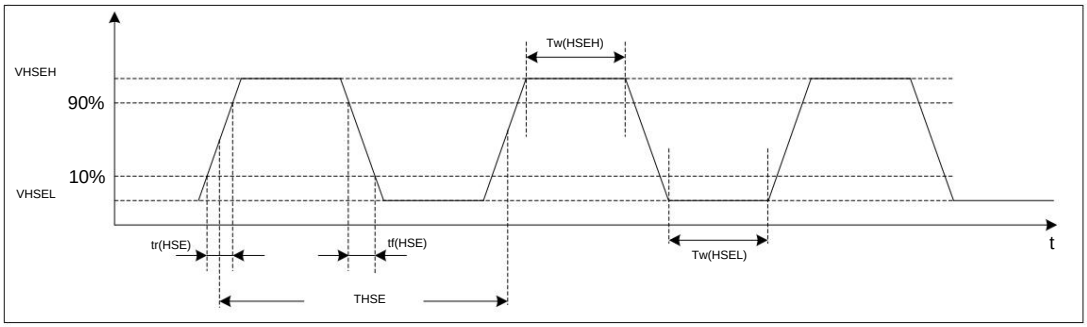


Figure 6-1 External high-speed clock timing diagram

Table 6-11 External high-speed clock characteristics

Symbol	**Parameter(1)**	Minimum value	Typical value	Maximum value	Unit
fHSE_ext	User external clock	0	8	32	MHz
VHSEH	frequency input pin high level	0.7VCC		VCC	V
VHSEL	voltage input pin low level voltage	Vss		0.3VCC	
tW(HSEH) tW(HSEL)	Enter high or low time	15			ns
tr(HSE) tf(HSE)	Enter rise/fall time	-		20	ns

(1) Guaranteed by design, not tested in production.

6.3.6.2.External high-speed crystal

It can be connected to an external 4~32MHz crystal/ceramic resonator. In the application, the crystal and load capacitor should be as close as possible to the pins so that Minimize output distortion and startup settling time.

Table 6-12 External high-speed crystal characteristics

Symbol	parameter	**Condition(1)**	**Minimum value (2)**	Typical value	**Maximum value (2)**	Unit
fOSC_IN oscillation frequency		-	4		32	MHz
IDD(4)	HSE power consumption	During startup			5.5	mA
		VCC=3V,Rm=30ÿ, CL=10pF@8MHz		0.58		
		VCC=3V,Rm=45ÿ, CL=10pF@8MHz		0.59		
		VCC=3V,Rm=30ÿ, CL=5pF@32MHz		0.89		
		VCC=3V,Rm=30ÿ, CL=10pF@32MHz		1.10		
		VCC=3V,Rm=30ÿ, CL=20pF@32MHz		1.90		
tSU(HSE)(3) (4)	Startup time	fOSC_IN=32MHz		3		ms
		fOSC_IN=4MHz		15		ms

(1) Crystal/ceramic resonator characteristics are based on the data sheet given by the manufacturer.

(2) Guaranteed by design, not tested in production.

(3) tSU(HSE) is the start-up time from enabling (via software) to clock oscillation reaching stability, measured for a standard crystal/resonator, different crystals Body/resonator can vary significantly.

(4) The data is based on assessment results and is not tested in production.

6.3.7. Internal high-frequency clock source **HSI** characteristics

Table 6-13 Internal high-frequency clock source characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
fHS	HSI frequency	TA=25°C,VCC=3.3V	23.83(2)	twenty four	24.17(2)	MHz
			21.97(2)	22.12	22.27(2)	MHz
			15.89(2)	16	16.11(2)	MHz
			7.94(2)	8	8.06(2)	MHz
			3.97(2)	4	4.03(2)	MHz
ÿTemp(HSI)	HSI frequency temperature drift	VCC=1.7V~5.5V, TJ=0C~85C	-2 (2)		2 (2)	%
		VCC=1.7V~5.5V, TJ=-40C~85C	-4 (2)		2 (2)	%
fTRIM(1)	HSI trimming accuracy			0.1		%
DHSI(1)	duty cycle		45 (1)		55 (1)	%
tStab(HSI)	HSI stabilization time			2	4 (1)	us
IDD(HSI) (2)	HSI power consumption	4MHz		100		uA
		8MHz		105		uA
		16MHz		150		uA
		22.12MHz, 24MHz		180		uA

(1) Guaranteed by design, not tested in production.

(2) The data is based on assessment results and is not tested in production.

6.3.8. Internal low-frequency clock source **LSI** characteristics

Table 6-14 Internal low-frequency clock characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
ikB	LSI frequency	TA=25°C,VCC=3.3V	-1		+1%	
ÿTemp(LSI)	LSI frequency temperature drift	VCC=1.6V~5.5V TJ=0C~70C	-10(2)		10(2)	%
		VCC=1.6V~5.5V,TJ=-40C~85C -20 (2)			20 (2)	%
fTRIM(1)	LSI fine-tuning			0.2		%
accuracy tStab(LSI) (1)	LSI stabilization time			150		us
IDD(LSI) (1)	LSI power consumption			210		nA

(1) Guaranteed by design, not tested in production.

(2) The data is based on assessment results and is not tested in production.

6.3.9. Memory characteristics

Table 6-15 Memory characteristics

symbol	parameter	condition	Typical	**Maximum (1)**	unit

tprog	Page program	-	1.0	1.5	ms
tERASE	Page/sector/mass erase -		3.0	4.5	ms
IDD	Page programe		2.1	2.9	mA
	Page/sector/mass erase		2.1	2.9	mA

(1) Guaranteed by design, not tested in production.

Table 6-16 Memory erase and write times and data retention

symbol	parameter	condition	**Minimum value (1)**	unit
NEND	Number of erases	TA = -40~85ÿ	100	kcycle
tRET	and writes Data retention period	10 kcycle TA = 55ÿ	20	Year

(1) The data is based on assessment results and is not tested in production.

6.3.10. **EFT** characteristics

symbol	parameter	condition	Grade typical value	unit
EFT to IO		IEC61000-4-4	B	2	KV
EFT to Power		IEC61000-4-4	B	4	KV

6.3.11. **ESD & LU** characteristics

Table 6-17 ESD & LU characteristics

symbol	parameter	condition	Typical value	units
VESD (HBM) static discharge voltage (human body model)		ESDA/JEDEC JS-001-2017	6	KV
VESD(CDM) static discharge voltage (charging equipment model)		ESDA/JEDEC JS-002-2018	1	KV
VESD(MM) Static Discharge Voltage (Machine		JESD22-A115C	200	V
LU	Model) Static Latch-Up	JESD78E	200	mA

6.3.12.**Port** characteristics

Table 6-18 IO static characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
VIH input high level voltage		VCC=1.7V~5.5V	0.7VCC			V
VIL input low level voltage		VCC=1.7V~5.5V			0.3VCCV	
Vhys(1) Schmidt hysteresis voltage				200		mV
Ilkg input leakage current					1	uA
RPU pull-up resistor			30	50	70	kÿ
RPD pull-down resistor			30	50	70	kÿ
CIO(1) pin capacitance				5		pF

(1) Guaranteed by design, not tested in production.

Table 6-19 Output voltage characteristics

symbol	**Parameter(1)**		Minimum value	Maximum value	unit
VOL	COM IO output low level	Conditions IOL = 8 mA, VCC ÿ	-	0.4	V
VOL		2.7 V IOL = 4 mA, VCC = 1.8 V	-	0.5	V

VOH	COM IO output high level	IOH = 8 mA, VCC ÿ 2.7 V	VCC–0.4	-	V
VOH		IOH = 4 mA, VCC = 1.8 V	VCC–0.5	-	V

(1) IO types can refer to the terms and symbols defined by the pins.

6.3.13. NRST pin characteristics

Table 6-20 NRST pin characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
VIH	input high level voltage	VCC=1.7V~5.5V	0.7VCC			V
VIL	input low level voltage	VCC=1.7V~5.5V			0.2VCCV	
Vhys(1)	Schmidt hysteresis voltage			300		mV
Ilkg	input leakage current				1	uA
RPU (1)	pull-up resistor		30	50	70	kÿ
RPD (1)	pull-down resistor		30	50	70	kÿ
CIO	pin capacitance			5		pF

(1) Guaranteed by design, not tested in production.

6.3.14. ADC characteristics

Table 6-21 ADC characteristics

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
IDD	power consumption	@0.75MSPS		1.0		mA
CIN(1)	internal sample and hold capacitor			5		pF
FADC	Conversion clock frequency	VCC=1.7~2.3V	1	4	6 (2) MHz	
		VCC=2.3~5.5V	1	8	12(2) MHz	
Tsamp(1)		VCC=1.7~2.3V	0.2			us
		VCC=2.3~5.5V	0.1			us
Tconv(1)				12*Tclk		
Teoc(1)				0.5*Tclk		
DNL(2)				±2		LSB
INL(2)				±3		LSB
Offset(2)				±2		LSB

(1) Guaranteed by design, not tested in production.

(2) The data is based on assessment results and is not tested in production.

6.3.15. Comparator characteristics

Table 6-22 Comparator characteristics (1)

symbol	parameter	condition	Minimum value	Typical value	Maximum value	Unit
VIN	Input voltage range		0		VCC V	
VBG	Scale input voltage		VREFINT			V
VSC	Scaler offset voltage			±5	±10 mV	
IDD(SCALER)	Scaler static consumption			0.8	1	uA
tSTART_SCALER	Scaler startup time			100	200	us
tSTART	Startup time to reach propagation delay specification	High-speed mode			5	us
		Medium-speed mode			15	
tD	Propagation delay	200mV step; High-speed mode		40	70	ns

		100mV over-drive	Medium-speed mode		0.9	2.3	us
		>200mV	High-speed mode			85	ns
		step;100mV overdrive	Medium-speed mode			3.4	us
Voffset	Offset error				±5		mV
Vhys	hysteresis	No hysteresis			0		mV
		With hysteresis			20		
IDD	consumption	Medium-speed mode; No deglitcher	Static		5		uA
			With 50kHz and ±100mv over-drive square sig-nal		6		uA
		Medium-speed mode; With de-glitcher	Static		7		uA
			With 50kHz and ±100mv over-drive square sig-nal		8		uA
		High-speed mode; No deglitcher	Static		250		uA
			With 50kHz and ±100mv over-drive square sig-nal		250		uA

(1) Guaranteed by design, not tested in production.

6.3.16.Temperature sensor characteristics

Table 6-23 Temperature sensor characteristics

symbol	parameter	Minimum value	Typical value	Maximum value	Unit
TL (1)	VTS linearity with temperature		±1	±2	ÿ
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/ÿ
V30	Voltage at 30ÿ(±5ÿ)	0.742	0.76	0.785	V
tSTART(1)	Start-up time entering in continuous mode		70	120	us
tS_temp(1)	ADC sampling time when reading the tempera-ture	9			us

(1) Guaranteed by design, not tested in production.

(2) The data is based on assessment results and is not tested in production.

6.3.17. Built-in reference voltage characteristics

Table 6-24 Built-in reference voltage characteristics

symbol	parameter	Minimum value	Typical value	Maximum value	Unit
VREFINT	Internal reference voltage	1.17	1.2	1.23	V
Tstart_vrefint	Start time of internal reference voltage		10	15	us
Tcoeff	Temperature coefficient			100(1)	ppm/ÿ
ivc	Current consumption from VCC		12	20	uA

(3) Guaranteed by design, not tested in production

6.3.18.Timer characteristics

Table 6-25 Timer characteristics

symbol	parameter	condition	minimum value	maximum value	unit
tres(TIM)	Timer resolution time	-	1		tTIMxCLK
		fTIMxCLK = 32MHz	20.833		ns
fEXT	Timer external clock frequency on CH1 to CH4	-		fTIMxCLK/2	MHz
		fTIMxCLK = 32MHz		twenty four	
ResTIM	Timer resolution	TIM1/3/14/16/17		16	Bit
tCOUNTER	16-bit counter clock period		1	65536	tTIMxCLK
		fTIMxCLK = 32MHz	0.020833	1365	us

Table 6-26 LPTIM characteristics (clock selection LSI)

prescaler	**PRESC [2:0]**	Minimum overflow value	Maximum overflow value	unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 6-27 IWDG characteristics (clock selection LSI)

prescaler	**PR[2:0]**	Minimum overflow value	Maximum overflow value	unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 6-28 WWDG characteristics (clock selection 32MHz PCLK)

prescaler	**WDGTB[1:0]**	Minimum overflow value	Maximum overflow value	unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

6.3.19. Communication port characteristics

6.3.19.1. I2C bus interface characteristics

The I2C interface meets the requirements of the I2C-bus specification and user manual:

ÿStandard-mode(Sm): 100kbit/s

ÿ Fast-mode(Fm): 400kbit/s

The timing is guaranteed by design, provided that the I2C peripherals are configured correctly and the I2C CLK frequency is greater than the minimum value required in the table below.

Table 6-29 Minimum I2C CLK frequency

symbol	parameter	condition	minimum value	unit
fI2CCLK(min)	Minimum I2CCLK freq uency	Standard-mode	**2**	MHz
		Fast-mode	9	

The I2C SDA and SCL pins have analog filtering capabilities, see the table below.

Table 6-30 I2C filter characteristics

symbol	parameter	Minimum value	Maximum value	unit
tAF	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

6.3.19.2. Serial peripheral interface **SPI** characteristics

Table 6-31 SPI characteristics

symbol	parameter	condition	minimum value	maximum value	unit
fSK 1/tc(SCK)	SPI clock fre- quency	Master mode	-	8	MHz
		Slave mode	-	8	
tr(SCK) tf(SCK)	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
tsu(NSS)	NSS setup time Slave mode		4Tpclk	-	ns
th(NSS)	NSS hold time	Slave mode	2Tpclk+10	-	ns
tw(SCKH) tw(SCKL)	SCK high and low time	Master mode, fPCLK = 36 MHz, presc = 4	Tpclk*2 -2	Tpclk*2 + 1	ns
tsu(MI) tsu(SI)	Data input setup time	Master mode, fPCLK = 48 MHz, presc = 4	Tpclk+5(1)	-	ns
		Slave mode, fPCLK = 48 MHz, presc = 4	5	-	
th(MI)	Data input hold time	Master mode	5	-	ns
th(SI)		Slave mode	Tpclk+5	-	
ta(SO)	Data output ac- cess time	Slave mode, presc = 4	0	3Tpclk	ns
tdis(SO)	Data output dis- able time	Slave mode	2Tpclk+5	4Tpclk+5	ns
tv(SO)	Data output valid im	Slave mode (after ena-ble edge), presc = 4	0	1.5Tpclk(2)	ns
tv(MO)	Data output valid im	Master mode (after en-able edge)	-	6	ns
th(SO)	Data output hold time	Slave mode, presc = 4	0 (3)	-	ns
th(MO)		Master mode	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

(1) Master generates 1pclk reception control signal before the reception edge.

(2) Slave has a maximum delay of 1PCLK based on the SCK sending edge. Considering IO delay, etc., 1.5PCLK is defined.

(3) When the SCK duty cycle sent by the Master is wide between the receiving edge and the sending edge, the Slave updates the data before the sending edge.

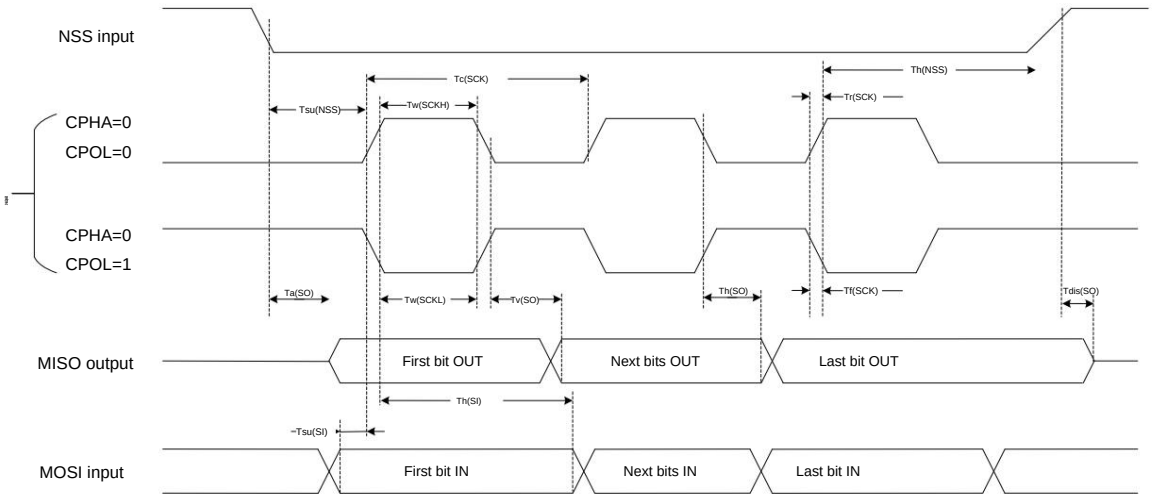


Figure 6-2 SPI timing diagram–slave mode and CPHA=0

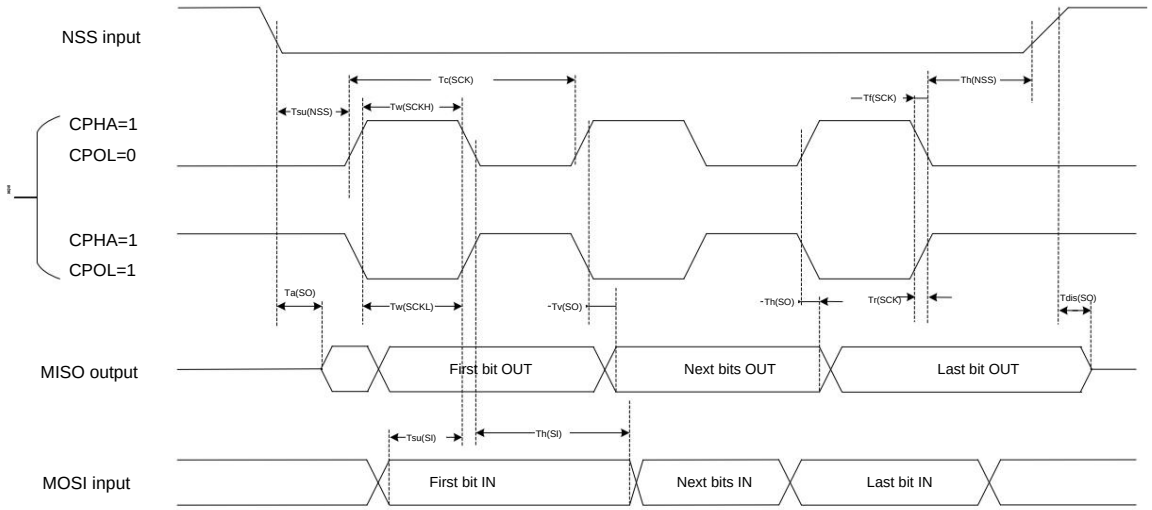


Figure 6-3 SPI timing diagram–slave mode and CPHA=1

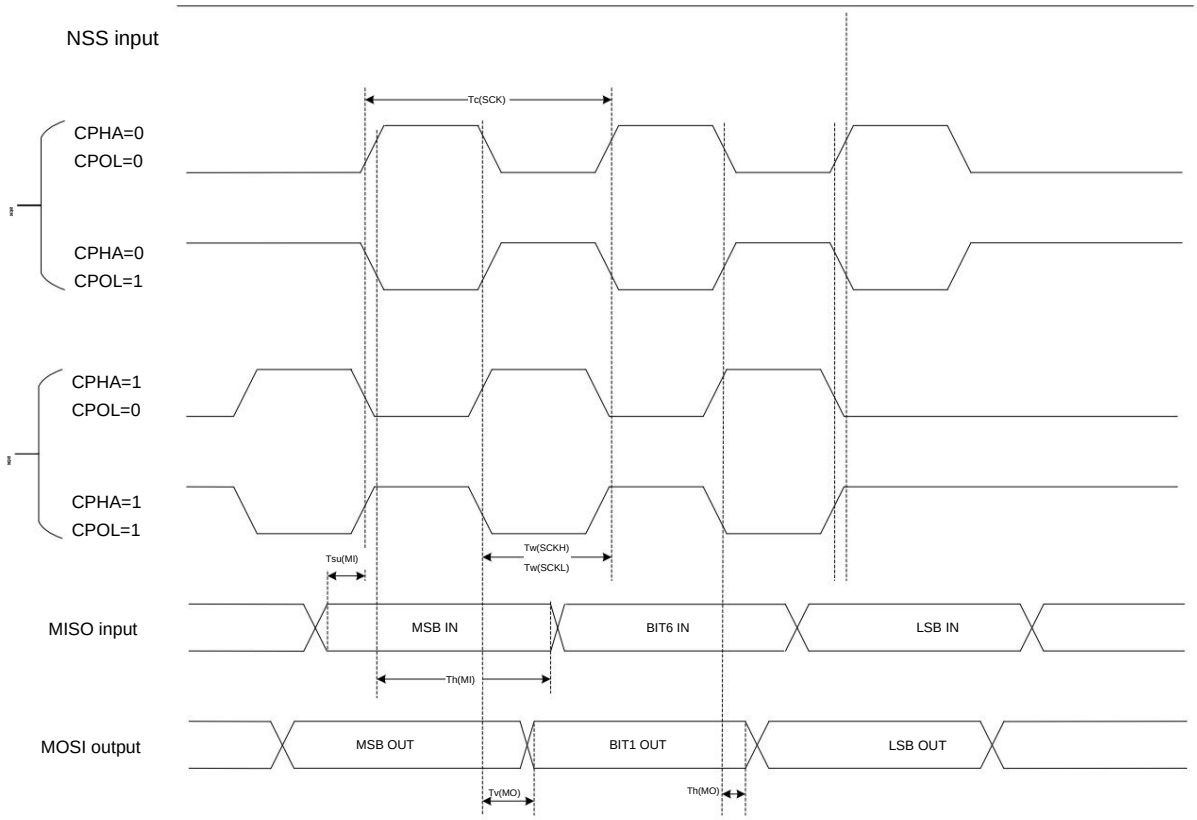
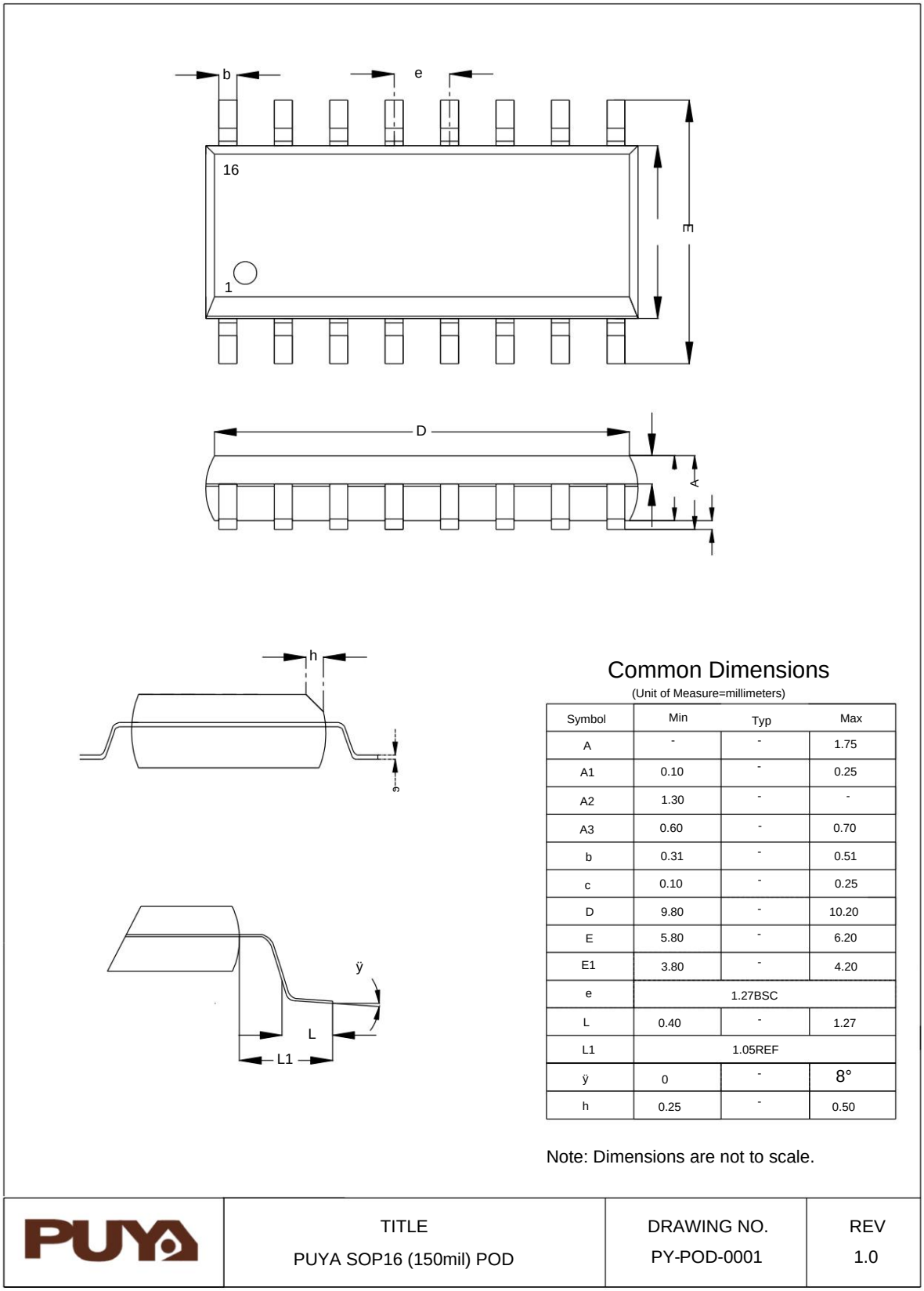


Figure 6-4 SPI timing diagram–master mode

7.Package information

7.1. **SOP16** package size



Common Dimensions

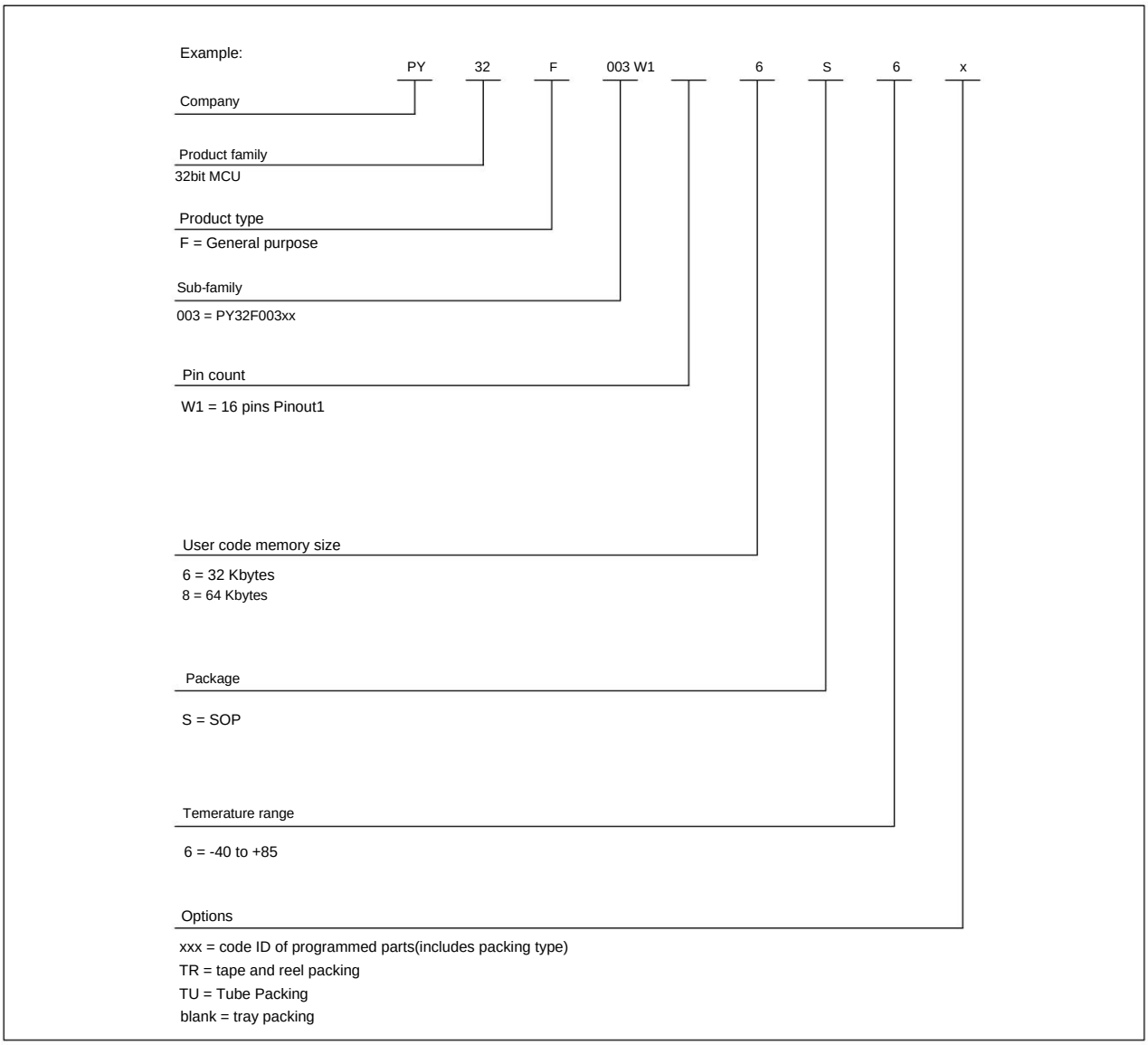
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	-	-
A3	0.60	-	0.70
b	0.31	-	0.51
c	0.10	-	0.25
D	9.80	-	10.20
E	5.80	-	6.20
E1	3.80	-	4.20
e	1.27BSC		
L	0.40	-	1.27
L1	1.05REF		
ÿ	0	-	8°
h	0.25	-	0.50

Note: Dimensions are not to scale.

	TITLE	DRAWING NO.	REV
PUYA	PUYA SOP16 (150mil) POD	PY-POD-0001	1.0

8.Ordering information



9. Version history

Version	date	update record
V0.1	2022.6.27 First edition	
V0.2	2022.7.5	New model PY32F003Wx8S

Puya Semiconductor Co., Ltd.